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(54) **Integrated piezoresistive pressure sensor and relative fabrication method**

(57) The pressure sensor is integrated in a SOI (Silicon-on-Insulator) substrate using the insulating layer as a sacrificial layer, which is partly removed by chemical etching to form the diaphragm. To fabricate the sensor, after forming the piezoresistive elements (10) and the electronic components (4, 6-8) integrated in the same chip, trenches (26) are formed in the upper wafer (23) of the substrate and extending from the surface to the layer of insulating material (22); the layer of insulating material (22) is chemically etched through the trenches (26) to form an opening (31) beneath the diaphragm (27); and a dielectric layer (25) is deposited to outwardly close the trenches (26) and the opening (31). Thus, the process is greatly simplified, and numerous packaging problems eliminated.
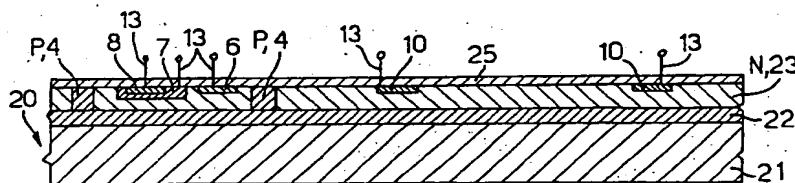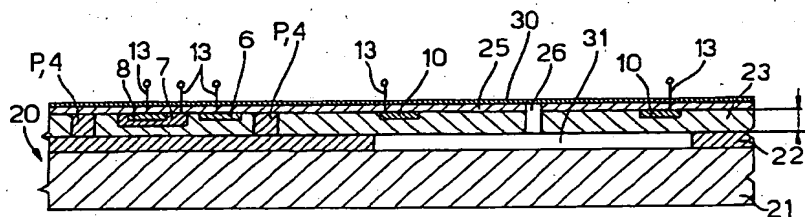
Fig. 2a

Fig. 2c

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Description

The present invention relates to an integrated piezoresistive pressure sensor and relative fabrication method.

As is known, in recent years, micromachining techniques have been developed for producing integrated micro pressure sensors of semiconductor material, which present numerous advantages as compared with traditional sensors: low cost; high degree of performance and reliability; better signal/noise ratio; integration with memory circuits for producing intelligent sensors; on-line self-testing; and greater reproducibility. As such, integrated micro pressure sensors are now being used increasingly in the automotive industry, in which they provide for greater safety and environmental protection with absolutely no increase in vehicle cost.

Currently marketed semiconductor micro pressure sensors are substantially based on two physical effects: a piezoresistive effect whereby the pressure-induced inflection of a silicon diaphragm unbalances a Wheatstone bridge comprising resistors diffused in the diaphragm; and a capacitive effect whereby pressure induces a shift in the position of a diaphragm forming the movable electrode of a capacitor (thus resulting in a variation in capacitance).

The present invention relates to a sensor implementing the first effect, i.e. to a piezoresistive sensor.

At present, diaphragms of semiconductor material (silicon) are produced using the bulk micromachining technique, which is described in detail, for example, in Articles "CMOS Integrated Silicon Pressure Sensor" by T. Ishihara, K. Suzuki, S. Suwazono, M. Hirata and H. Tanigawa, IEEE Journal Sol. St. Circuits, vol. sc-22, Apr. 1987, 151-156, and "Micromachining and ASIC Technology" by A.M. Stoffel, Microelectronics Journal 25 (1994) 145-156.

For the sensor to operate effectively, the diaphragms must be of uniform, accurately controlled thickness with no intrinsic mechanical stress, which characteristics are achieved by forming the microstructures by plasma or wet etching, isotropic etching (for profiles coincident with the crystal faces) or anisotropic etching (for more sharply curved, continuous profiles). At present, the best etching method for producing the diaphragm, and which provides for more accurately controlling the thickness of the diaphragm and eliminating any process-induced tensile or compressive stress, is the electrochemical stop method using a PN junction whereby the diaphragm is formed in an N-type monocrystalline semiconductor layer (e.g. the epitaxial layer) on a P-type substrate; the N-type layer is masked except for a previously implanted anode contact region; the rear of the substrate is masked with a mask presenting a window aligned with the region in which the diaphragm is to be formed; a positive potential difference is applied between the N-type layer and the substrate via the anode contact region; and the P-type substrate is

chemically etched for a few hours at low temperature (e.g. 90°C). Etching terminates automatically at the PN junction, and the N-type layer at the removed substrate region forms the diaphragm.

An example of the fabrication steps of an absolute piezoresistive micro pressure sensor using the electrochemical stop method is described below with reference to Figures 1a, 1b and 1c.

The initial steps are those commonly adopted in the fabrication of integrated circuits. That is, commencing with a wafer 1 of monocrystalline silicon comprising a P-type substrate 2 and an N-type epitaxial layer 3, P-type junction isolating regions 4 extending from the upper surface of wafer 1 to substrate 2 are formed in epitaxial layer 3; the integrated circuit is then formed (Figure 1a shows an NPN transistor with an N$^+$ type collector contact region 6, a P-type base region 7, and an N$^+$ type emitter region 8); and, simultaneously with the integrated circuit, the diffused resistors (only one of which, comprising a P-type resistive layer 10, is shown) and one anode region for each wafer and each diaphragm (N$^+$ type region 11 in Figure 1a) are formed. The resistors are preferably formed in the same step in which base region 7 of the NPN transistor is implanted; and anode region 11 is formed in the same step as one of the N-type regions of the integrated circuit (e.g. when implanting collector contact region 6 or emitter region 8). A dielectric layer 12 is then deposited, and metal contacts 13 formed.

At this point, wafer 1 is masked with a front mask 15 and a rear mask 16, the front mask 15 (of silicon oxide) covering the whole of the upper surface of wafer 1 except for a window at anode region 11, and the rear mask 16 (of silicon nitride or oxide) covering the whole of the lower surface of the wafer except for the region in which the diaphragm is to be formed, as shown in Figure 1b. The rear of the wafer is then subjected to anisotropic etching; at the same time, epitaxial layer 3 is biased, via anode region 11, at a positive voltage (e.g. 5V) with respect to substrate 2. Anisotropic etching terminates automatically at epitaxial layer 3; and the portion of epitaxial layer 3 at the removed portion of substrate 2 forms the diaphragm 18.

Following removal of masks 15 and 16, wafer 1 is bonded to a sheet of glass 17 (Figure 1c) using the anodic bonding method whereby a medium-high voltage (e.g. 500 V) is applied between wafer 1 and sheet 17 for a few hours at a temperature of 300 to 400°C; and, finally, sheet 17 is fixed to container 19.

The above method presents the following drawbacks: it is incompatible with batch processing techniques, due to the electric contacts on each wafer; rear etching of wafer 1 poses problems in terms of front-rear alignment; the thickness of wafer 1 demands prolonged etching; the scaling problems involved are such as to preclude the integration of structures smaller than a few hundred micrometers; and, once the diaphragm is formed, wafer 1 must invariably be bonded to a glass

support, both for absolute and differential sensors (which require holes aligned with the diaphragm, thus posing further alignment problems).

On account of the above drawbacks, which make it difficult to integrate the method in currently used integrated circuit technology, several micro pressure sensor manufacturers have opted to form an integrated double chip: one chip contains the diaphragm microstructure, while the other provides for processing the signal. Single-chip integrated sensors also exist, but are not batch processed.

Several industrial laboratories and research centers have produced prototype integrated microstructures using the surface micromachining technique. Details of these are to be found, for example, in the following Articles: "Novel fully CMOS-compatible vacuum sensor", by O. Paul, H. Baltes, in Sensors and Actuators A 46-47 (1995) p. 143-146, in which a diaphragm of dielectric material is formed on a sacrificial metal layer; "Surface-Micromachined Piezoresistive Pressure Sensor" by T. Lisec, H. Stauch, B. Wagner, in Sensor 95 Kongressband, AO1.2, p. 21-25, in which both the sacrificial layer and the diaphragm are of polysilicon and separated by a small layer of silicon oxide; and "Surface-Micromachined Microdiaphragm Pressure Sensors" by S. Sugiyama, K. Shimaoka, O. Tabata, in Sensors and Materials 4, 5 (1993), p. 265-275, in which use is made of a sacrificial polysilicon layer and a silicon nitride layer as the diaphragm.

Though they do in fact provide for better integrating the devices, the above surface micromachining techniques pose serious problems as regards the quality of the films (amorphous or polycrystalline) deposited to form the diaphragms, collapse of the suspended structures on the silicon substrate, and packaging difficulties.

It is an object of the present invention to provide an integrated piezoresistive sensor and relative fabrication method, designed to overcome the aforementioned drawbacks.

According to the present invention, there are provided an integrated piezoresistive pressure sensor and relative fabrication method, as claimed respectively in Claims 1 and 9.

In practice, according to the present invention, the sensor exploites a SOI (Silicon-on-Insulator) substrate to form the diaphragm, and the insulating layer forms the sacrificial layer removed partly by chemical etching to form the diaphragm, thus greatly simplifying the process and eliminating many of the packaging problems involved.

Two preferred, non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figures 1a, 1b and 1c show cross sections of a wafer of semiconductor material at successive steps in the fabrication of a known sensor;

Figures 2a, 2b and 2c show cross sections of a wafer of semiconductor material at successive steps in the fabrication of the sensor according to the present invention;

Figure 3a shows a top plan view of a detail of the sensor according to the present invention;

Figure 3b shows a top plan view of a different embodiment of the sensor according to the present invention.

The sensor according to the present invention is formed from a SOI substrate formed in known manner. In the Figure 2a example, the SOI substrate forms a wafer 20 comprising an actual substrate region 21 of monocrystalline silicon of any conductivity type (P or N) superimposed with an, e.g. SiO_2, insulating layer 22 deposited or grown thermally, and to which a monocrystalline silicon layer 23, in this case an N-type, is bonded in known manner (e.g. as described in the Article entitled "Silicon-on-Insulator Wafer Bonding-Wafer Thinning Technological Evaluations" by J. Hausman, G.A. Spierings, U.K.P. Bierman and J.A. Pals, Japanese Journal of Applied Physics, Vol. 28, N. 8, August 1989, p. 1426-1443). The thickness of insulating layer 22 is preferably 600 to 1200 nm. The thickness of the second wafer 23 depends, as explained below, on the full scale pressure of the sensor, diaphragm size and fabrication parameters, and roughly ranges between 5 and 10 µm.

As of wafer 20, the standard fabrication steps described above are performed to form junction isolating regions 4, the integrated electronic components (regions 6-8) and diffused P-type piezoresistors 10, but, unlike the known method, anode region 11 is not formed.

At this point, according to the method of the present invention, the upper face is covered with a deposited plasma nitride layer (layer 25 in Figure 2a), which acts as a first passivation layer and as a mask for forming trenches in second wafer 23. Nitride layer 25 is etched photolithographically and provides, at a subsequent etching step, for forming a number of trenches 26 in second wafer 23, as shown in Figures 3a and 3b.

Wafer 20 is then etched with hydrofluoric acid, which penetrates trenches 26 in second wafer 23 to remove part of buried insulating layer 22 and form an opening or window 31 in layer 22, so that the portion of second wafer 23 over opening 31 forms the diaphragm 27. By appropriately regulating the etching time of insulating layer 22 and the location of trenches 26, diaphragm 27 may be shaped and sized as required, and more specifically in such a manner as to ensure piezoresistors 10 are located at the edges of diaphragm 27, i.e. in the maximum pressure-induced stress region. Figure 3a, for example, shows a first embodiment in which the diaphragm (27a) is circular, and trenches 26 are formed at the center of the diaphragm, inside a circle 28 concentric with circle 27a. In a second embodiment shown in Figure 3b, the diaphragm (27b) is square and trenches 26 arranged appropriately.

At this point, a dielectric (e.g. USG - Silicon Glass) layer 30 is deposited to cover the top of trenches 26, insulate trenches 26 and opening 31 (Figure 2c), and so eliminate the anodic bonding step called for in the bulk micromachining method. The wafer 20 so formed may then be subjected to the usual finish operations - comprising cutting, packaging and direct connection of the die to the container - with no alterations as compared with standard IC processes.

The size of diaphragm 27 and circle 28 (trench region) typically depend on the pressure measuring range according to the equations shown below.

In the Figure 3a embodiment - in which diaphragm 27a is circular with a radius $\underline{a}$, circle 28 presents a radius $\underline{b}$, and pressure P is evenly distributed over the surface - maximum stress S_{max} and maximum vertical deflection W_{max} equal:

$$S_{max} = k\,P\,(a/s)^2$$

$$W_{max} = h\,P\,(a^4/Es^3) \qquad (1)$$

where $\underline{s}$ is the thickness of the diaphragm (thickness of second wafer 23, Figure 2c); E is the Young's modulus of monocrystalline silicon (130 GPascals); and $\underline{k}$ and $\underline{h}$ are numbers depending on how the diaphragm is anchored and on ratio a/b. For ratio a/b values of 1.25 to 5, $\underline{k}$ ranges between 0.1 and 0.73, and $\underline{h}$ between 0.002 and 0.17.

Bearing in mind that the maximum stress withstandable by silicon is roughly 4000 bars, and if Q is the full scale pressure of the sensor in bars, the following equation applies:

$$(a/s)^2 = 0.8^*10^3/(k^*Q)$$

Conversely, in the case of a square diaphragm of side 2a (Figure 3b) and with no change in the other parameters, equation (1) equals:

$$W_{max} = h\,P\,(a^4/Es^3)/3 \qquad (1')$$

The advantages of the sensor and fabrication method described are as follows: the fabrication method is compatible with batch processing, and therefore provides for exploiting the same economic advantages; the sensor may be fully integrated with the signal processing circuit, so that the sensor and all the processing logic may be contained in one chip, thus reducing size, signal transmission time and sensitivity to external phenomena; no problems exist as regards front-rear alignment; spatial integration of the sensor is comparable with surface-micromachined structures and greater by one or two orders of magnitude as compared with bulk-micromachined sensors; by featuring a monocrystalline silicon diaphragm, the mechanical characteristics of the sensor are superior to those of deposited films typical of surface-micromachined structures; and, finally, by elim-

inating the need for a glass support, no anodic bonding is required.

Clearly, changes may be made to the sensor and fabrication method as described and illustrated herein without, however, departing from the scope of the present invention. In particular, the conductivity of the various regions may be other than as shown, e.g. the conductivity of the second wafer and the piezoelectric resistors may be dual; components of any type and compatible technology may be integrated in the structure; and isolating regions 4 may be of a type other than as shown, e.g. dielectric.

Claims

1. An integrated piezoresistive pressure sensor comprising a diaphragm (27; 27a; 27b) formed in a body of semiconductor material (20); and a number of piezoresistive elements (10) formed in said diaphragm; characterized in that said body of semiconductor material is a SOI substrate (20).

2. A sensor as claimed in Claim 1, characterized in that said body of semiconductor material (20) comprises a first wafer (21) of monocrystalline semiconductor material; a layer of insulating material (22) over said first wafer (21); and a second wafer (23) of monocrystalline semiconductor material over said layer of insulating material (22); said diaphragm (27; 27a; 27b) being formed in said second wafer (23) in a portion directly facing said first wafer (21) at an opening (31) in said layer of insulating material.

3. A sensor as claimed in Claim 2, characterized by at least one trench (26) formed in said second wafer (23), located at said diaphragm (27; 27a; 27b), and connected to said opening (31) in said layer of insulating material (22).

4. A sensor as claimed in Claim 3, characterized in that said at least one trench (26) is formed in a central portion of said diaphragm (27; 27a).

5. A sensor as claimed in Claim 3 or 4, characterized by a layer of dielectric material (25) for closing said at least one trench (26).

6. A sensor as claimed in any one of the foregoing Claims, characterized in that said diaphragm (27a) is circular.

7. A sensor as claimed in Claim 6, characterized in that said diaphragm (27a) presents a radius $\underline{a}$, and said second wafer (23) presents a thickness $\underline{s}$; and in that:

$$(a/s)^2 = 0.8^*10^3/(k^*Q)$$

where $\underline{k}$ is a process parameter, and Q is a full scale pressure of the sensor.

8. A sensor as claimed in any one of the foregoing Claims from 1 to 5, characterized in that said diaphragm (27b) is square.

9. A method of fabricating an integrated piezoresistive pressure sensor as claimed in any one of the foregoing Claims, characterized by the steps of:

   - forming a SOI substrate (20);
   - forming a diaphragm (27; 27a; 27b) in said SOI substrate; and
   - forming piezoresistive elements (10) in said diaphragm.

10. A method as claimed in Claim 9, characterized in that said step of forming a SOI substrate comprises the step of forming a body of semiconductor material (20) comprising a first wafer (21) of monocrystalline semiconductor material, a layer of insulating material (22) over said first wafer (21), and a second wafer (23) of monocrystalline semiconductor material over said layer of insulating material (22); and in that said step of forming a diaphragm (27; 27a; 27b) comprises the steps of:

    - forming at least one trench (26) through said second wafer and extending up to said layer of insulating material (22); and
    - forming an opening (31) in said layer of insulating material (22) by chemical etching through said at least one trench (26).

11. A method as claimed in Claim 10, characterized by the further step of depositing a layer of dielectric material (25) on said second wafer (23); said layer of dielectric material outwardly closing said at least one trench (26).

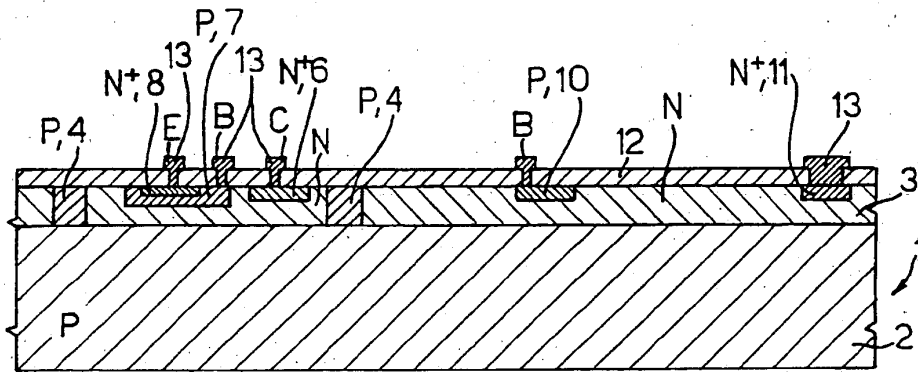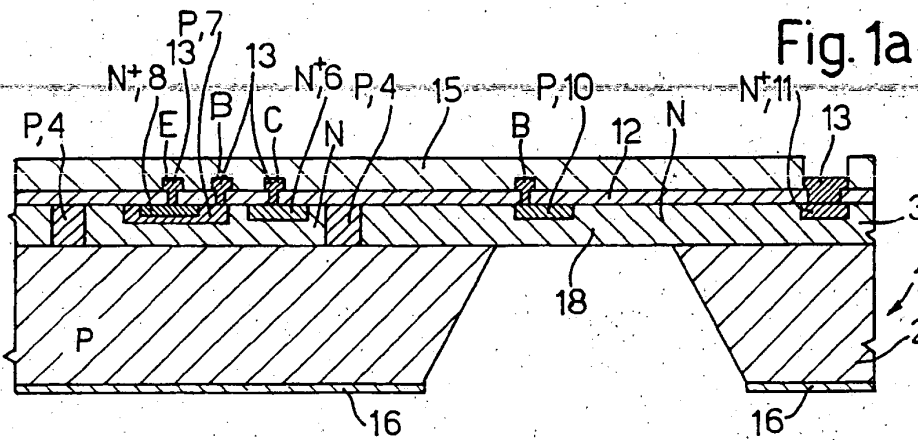12. A method as claimed in Claim 10 or 11, characterized by the step of bonding said body of semiconductor material (20) directly to a container.
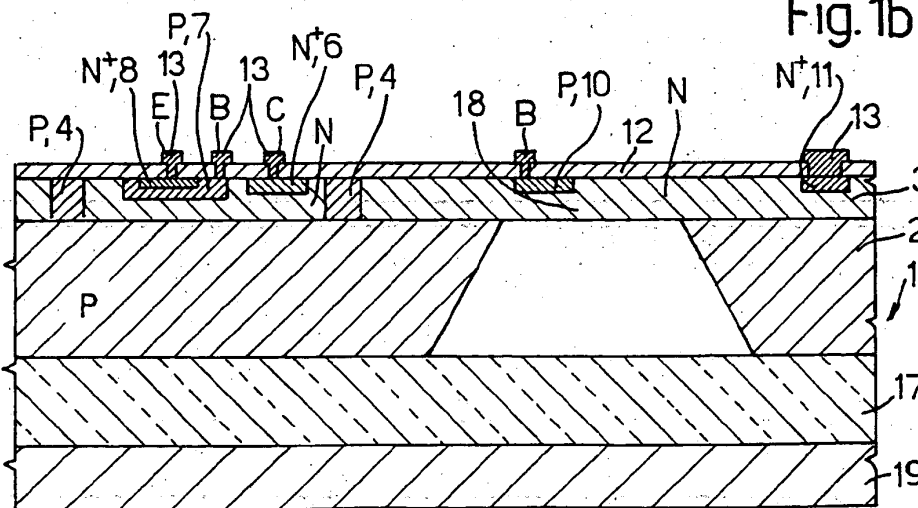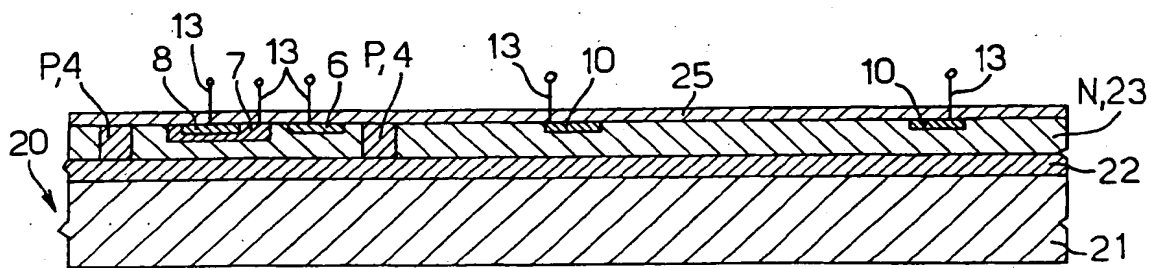
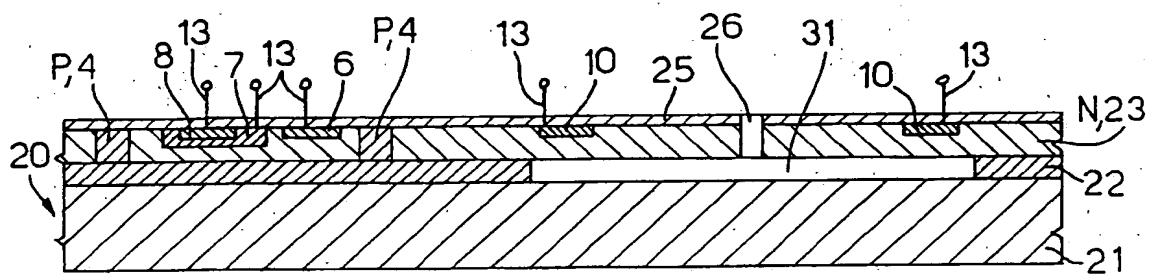Fig. 1a

Fig. 1b

Fig. 1c

Fig. 2a

Fig. 2b
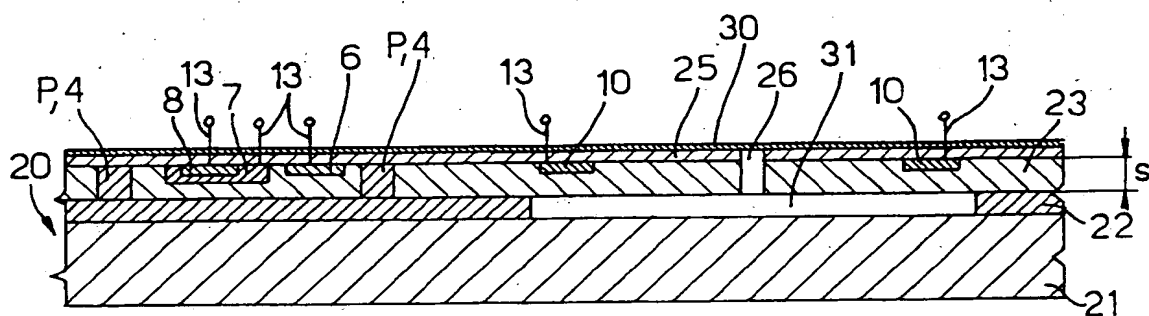
Fig. 2c
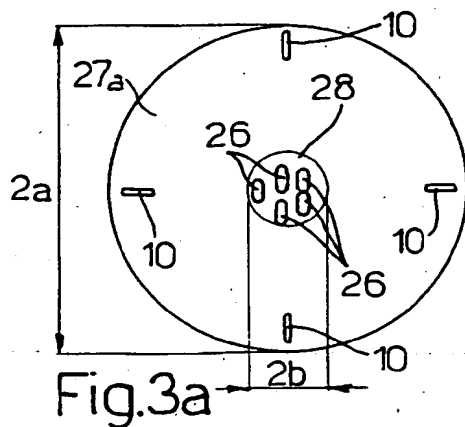
Fig. 3b

Fig. 3a
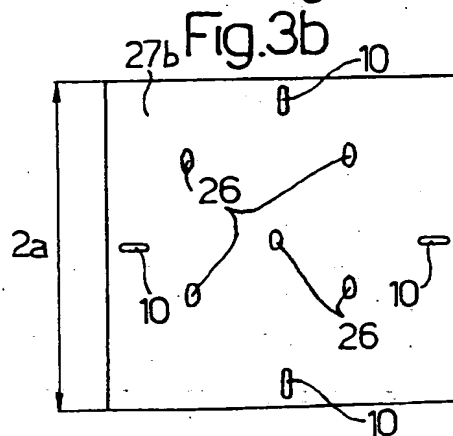
European Patent Office	EUROPEAN SEARCH REPORT	Application Number EP 96 83 0435

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 605 302 (COMMISSARIAT A L'ENERGIE ATOMIQUE) * the whole document * ---	1-6,9-11	G01L9/06
X	FR-A-2 201 464 (MOTOROLA, INC.) * the whole document * ---	1,8,9	
X	US-A-5 095 401 (P.M. ZAVRACKY ET AL.) * the whole document * ---	1,6,8,9	
X	US-A-4 766 666 (S. SUGIYAMA ET AL.) * the whole document * -----	1,9	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) G01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 December 1996	Van Assche, P

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